IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 14, Issue 4, Ser. I (Jul.-Aug. 2019), PP 27-38
www.iosrjournals.org

Implementation of Control Circuitry for Ultra-Low Power ROM

Riya Dey[1], Pamisetty Udayabhanu[2] , Neethu Johny[3]
[1,2]*B.E, Department of Electronics and Communication,New Horizon College of Engineering, Bangalore*
[3]*Asst.Prof, Department of Electronics and Communication,New Horizon College of Engineering, Bangalore-560103*
Corresponding Author; Riya Dey

Abstract-*Read-Only Memory (ROM) is a kind of storage medium that permanently stores the data on electronic devices. Almost all electronic devices have ROMthat containsprogramming which is essential for boot-up and also executing major I/O tasks and holds programs or software instructions. In today's world, low power is a very crucial aspect of any electronic device. People are constantly looking for devices with longer battery life. The ROM is being used in almost all electronic devices; a low power approach will make the device more efficient. The proposed paper introduces design techniques to reduce the power consumption in the control circuitry of a 128X128 ROM. The control circuitry consists of decoders, latches and clock. The proposed design of decoder has less number of transistors and consumes 61% less power compared to conventional designs. Clock gating has also been introduced for power reduction. SEM based latch was used to decrease the transient noise pulses.*

Keywords:*ROM, low-power, decoder, low phase latch, clock gating*

Date of Submission: 06-07-2019 Date of acceptance: 23-07-2019

I. Introduction

Moore's Law states that the number of transistors in a chip doubles every 18 to 24 months. The die area increases by 14% to satisfy Moore's Law. Also, the frequency doubles every two years. Since power is a function of die area and frequency, scaling of technology leads to about a 40% increase in the power density per generation. We are at a technological epoch where low power is of the ultimate demand. The growing market demand of portable devices like cellular mobiles, tablets, portable music devices like iPods and MP3 players, handheld gaming consoles, smart watches and electronic systems which are battery-powered demands microelectronic circuit design with ultra-low power dissipation and high throughput.In processor-based SoC, most of the time, they limit the speed [1].So, ROMs have to be designed to work at very low supply voltages and to be very robust while considering wire delays, signal input slopes, noise and crosstalk effects [1].

The control circuitry is a very important part of the ROM architecture. Reading of the data stored is initiated by the control circuitry. In conventional ROM architecture, control circuitry consumes about 20% of the overall powerhead. The control circuitry consists of the latches, column address decoder, row address or word-line decoder and clock to drive them. The conventional decoder is constructed using inverters and AND gates. However, this technique can pose a great demand for power with an increase in the dimensions of the ROM since the number of AND gates required will also increase. Latches used to hold the data also need to be optimized in order to reduce power.

To overcome the problems of high-power usage in ROM and in turn reduce the power consumption of electronic devices, a novel approach for the construction of the control circuitry of ROM using Cadence 180nm technology has been proposed here. Architectural changes have been made to the decoder (both word-line decoder and column decoder) in order to decrease the consumed power. Latch has also been designed for the above purpose.

The remainder of the paper is organized as follows. SectionII will describe the overall design of the control circuitry. Section III talks about clock gating. Section IV shows the proposed decoder design. Section V describes the low phase latch. The schematic and simulation results are shown in VI. Finally, section VII concludes the paper.

II. Control Circuitry

The control circuitry consists of decoders (address/wordline and column decoder), latches and also clock gating for power reduction. The proposed paper makes use of 128X128 dimension of MROM. For this, we need to provide a 7-bit address to access a memory location in this ROM. To create a 128X128 ROM we would require 128 wordlines and 128 bitlines. For these 128 wordlines and bitlines, we require a 7:128 decoder.

For each 7-bit binary address input, precisely only one of the 128 wordlines is triggered by the wordline or address decoder. Also, to hold the 7 address bits, 7 address latches are necessary.Once the 7-bit address is input, the gated clock is activated immediately. This is done by passing a logic 1 to the memory enable latch. The gated clock will further activate the address latches and the decoders. Next, the column and row decoders will activate the particular wordline and bitline as indicated by the 7-bit address.

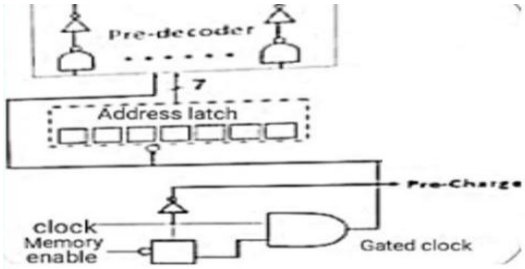

Fig. 1: Control circuitry diagram

III. Clock Gating

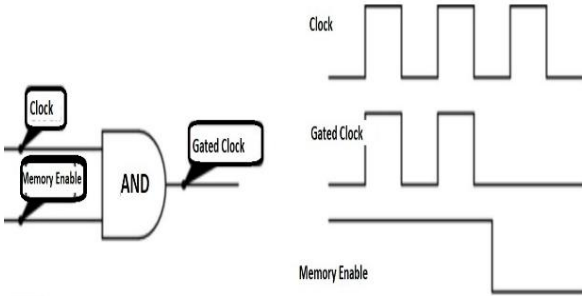

Fig. 2: Gated clock

The clock signal is the highest frequency signal toggling in any electronic device or SoC.Clock consumes about 60-70% of the total chip power. This is further predicted to increase exponentially in the designs of the next generations at 45nm and below. This is due to the fact that power is directly proportional to voltage and the frequency of the clock as shown in the below equation:

$$P_{\text{switching}} = \alpha C V_{DD}{}^2 f$$

Clocks continuously consume power because it toggles the FF or latch and their associated logic. So, to reduce power consumption clock gating turns off the clock when the system is maintaining its current state.Clock gating is a power-saving feature in semiconductor micro-electronics whichallows switching off of circuits. Clock gating decreases unwanted switching on some parts of the clock net by disabling the clock. The enable should setup before the clock. If not, the data will be corrupted.

To reduce the dynamic power consumption, clock gating is the most frequently used optimization technique.Clock gatingis very effective in reducing the power consumption in digital circuits and also in VLSI circuits. Countless electronic devices make use of clock gating to switch off controllers,buses, bridges, portions of processors, and also to reduce the dynamic power consumption in the circuits.However, thedifficulty of optimizing power by including clock gating is having proper knowledge of when and whereto insert the gating.

In our design, we have implemented the gated clock by making use of a simple CMOS AND gate. The two inputs of the AND gate is the Memory enable signal and the clock. Only when the memory enable signal is high, the clock signal will get passed to the output of the AND gate and the gated clock will be activated. On the other hand, if the memory enable signal is low, the AND gate output will be low, indicating that the gated clock is OFF. This has been clearly explained in Fig.2.

IV. Decoder

The decoder is one of the most important peripheral circuits for memory. The decoder is a combinational circuit that converts n coded inputs to a maximum of 2^k unique outputs. Decoder is used in memory circuits for selecting some particular wordline or bitline. The speed of the storage cell is directly proportional to the speed of the decoder.The decoder should be designed appropriately so that its size matches with the size of the memory cell and a memory wordline or bitline is selected by providing a binary encoded address (A0 to Ak-1). The decoder deciphers this address into the N=2k select lines, only one of which will be active at a particular time [2]. The row and column selection are done by row or wordline and column or bitline

decoder respectively. Row decoder is used to select the wordline while column decoder used to select the bitlines.

A. CONVENTIONAL DECODER

The conventional approach of constructing decoders makes use of AND gates. Fig. 3 shows a conventional binary logic line 2:4 decoder. Itcomprises of 2 inverters and 4 AND gates. The two binary inputs named A0 and A1 are decoded into one of four outputs, hence the description of 2:4decoder. Each output signifies one of the minterms of the two inputs. The binary inputs A0 and A1 regulate which output from D0 to D3 is "HIGH" (logic 1) while the remaining outputs are held "LOW" (logic 0). So only one of the outputs can be high(logic 1) at any one point of time. The majordrawback of using this method is that it takes up a much larger area due to the use of a large number of transistors. Around 48 transistors are needed in this method for a 2:4 decoder in static CMOS technology.

To implement a 7:128 decoder using AND gates is even more complicated. As the size of the decoder increases, the number of inputs to the AND gate also increases.For a k-bit to 2^k decoder, we need to create 2*kk-input AND gates. For 7:128 decoder, we will require 14 7-input AND gates. However, gates with more than 3 or 4 inputs tend to create large series resistance and experience more delay. Instead of using k-input gates, it is desirable to use a cascade of gates instead.

Typically, two stages are used: a pre-decode stage and a final decode stage. The pre-decoding stage produces intermediate signals that are then used by many gates in the final decode stage. The final decoding stage combines the intermediate results of the pre-decoding stage to generate the final output. The key advantage of two-level decoding is that a large number of intermediate signals can be created by the pre-decoding stage and then reused by the final decoding stage. This resultsin the reduction of the number of inputs to each gate.

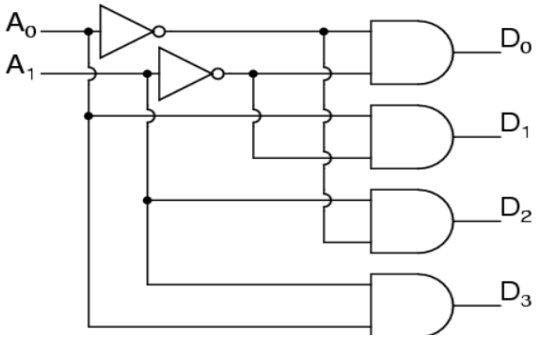

Fig. 3: Conventional decoder

B. PROPOSED DECODER DESIGN

Conventional methods use static CMOS circuit to implement the design of the decoder. However, the power dissipation is observed to be very high and the main reason behind thisincrease in power is becauseof the increase in the number of transistors. The mixed logic techniqueused to construct the decoder effectively reduces the transistor count which in turn results in lower power consumption. Since power consumption depends on the number of transistors that are active duringoperation, this drives a need to optimize the design for low power without forfeiting other performances characteristics. The foremostaim of this technique is to decrease the transistor count by discarding the redundant logic parts that arepresent in the conventional static CMOS circuits.

The mixed logic technique is one of the most reliable techniqueto crackthe solution of all combinational circuit synthesis problems. This method provides reduced power consumption and very little delay as compared to conventional CMOS techniques [4]. It alsoprovides a high-performance design which is driven by synthesis technique and PTL cell selection [5].

This mixed logic design technique can reduce the transistor count essential to construct a 2:4 decoder. It is termed mixed logic since it used two logics together: TGL (Transmission Gate Logic) logic and DVL (Dual Value Logic) logic. Todesign a 2:4 mixed logic decoder using TGL and DVL gates we would need a total of 16 transistors (12 for AND gates and 4 for inverters). However, by mixing both AND gate types (TGL AND gate and DVL AND gate) into the same design and by using an appropriatearrangement of signals, it is also possible to remove one of the two inverters. Doing this would reduce the total number of transistors needed to 14. Removing the inverter at input B reduces the number of transistors, which will reducethe logical effort andthereby essentially reducing the switching activity in the circuits. This, in turn,will reduce the power consumption significantly.The mixed logic line 2:4 decoder circuit is shown in Fig. 4. It can be seen that theinverter at input B is removed by realizing the outputs D0 and D2 withDVL AND gate, usingA as

propagating signal. Whereas, outputs D1 and D3 arerealized with TGL AND gate, using B as propagating signal. As a resultof this, the use of B complement is eliminated and thereforethe number of transistors is reduced to 14(5 PMOS and 9 NMOS transistors respectively).

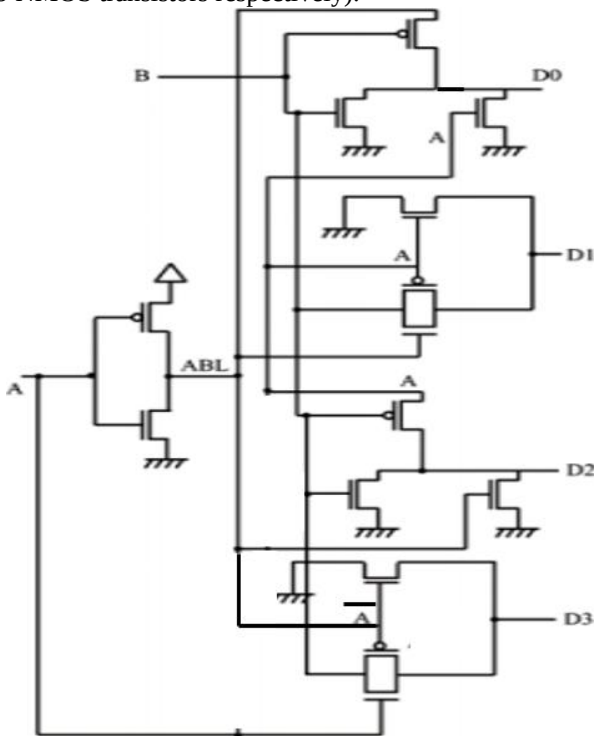

Fig. 4: Mixed logic 2:4 line decoder

C. PROPOSEED 7:128 DECODER

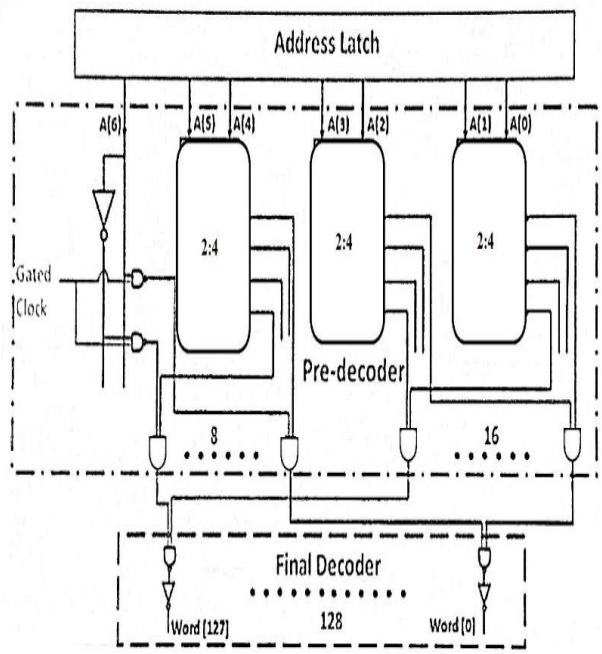

Fig. 5: 7:128 Decoder with clock gating

The 7:128 decoder designed by keeping clock gating in mind is shown in Fig. 5. This 7:128 decoder consisted of three 2:4 decoders which were constructed using mixed logic. The last address bit A6 (MSB), was combined with a gated clock using NAND gates. The two 2:4 mixed logic line decoders with inputs as A0, A1 and A2, A3 were combined together to form a 4:16 decoder. The other 2:4 mixed logic decoder with inputs A4, A5 and the MSB A6 which was incorporated with clock were combined together to form a 3:8 decoder. These

4:16 and 3:8 were then combined in the final decoder stage to form the 7:128 decoder. The advantage of this design is the incorporation of clock gating which strives to reduce the power consumption.

The number of AND gates required in the pre-decoding stage of 7:128 decoder with and without clock gating is 24. The 7:128 decoder with clock gating also requires two extra NAND gates which will increase the area of the design. However, while designing, out of the performance, power and area (PPA) any one will have to be compromised. Since the 7:128 decoder with clock gating has reduced power which is our main aim, we have used this design of the decoder.

V. Low Phase Latch

A latch is an electronic logic circuit which has two stable states. Latches have a feedback loop to hold the data. Therefore, a latch can be consideredas a memory unit.As long as the circuit is turned on, thelatch can store or hold one bit of data. On applying enable signal (active high or active low), the latch immediately updates the stored data as soon as the input is changed.

We have made use of D latch in our control block due to the fact that whatever be the input, the same will be reflected at the output.The latch is used in the control block for two applications. They are: Address latch and the Memory Enable latch. The Address latch is used to hold the address of the location from where the data needs to be read. Since we have a 7-bit address, we will require 7 Address latches each holding one address bit. The output of the Address latches is given to the inputs of the 7:128 decoders. The Memory Enable latch is essential to hold the memory enable bit. The memory enable bit is logic 1. This is used to activateclock gating. The output of the Memory Enable latch is given as an input to the AND gate or the gated clock.

A. WHY USE LATCH AND NOT FLIP-FLIP?

Latches and flip-flops are both basic sequential elements that are vital for several VLSI designs. The main reason for using a latch to store the data in our design of the control circuitry instead of a flip-flop is because latch will immediately update its output as soon as the input changes.Also, in the case of flip-flops the performance depends upon the longest combinational pathdelays. Iflatches are used instead, we can reimburse the longest combinational path delays by borrowing time from the shorter path delays in the subsequent stages. Using this we can decrease the delays and thereby raise the performance of the design.This property is called "Time-Borrowing" which is a major plus point of the latches. The latchesare also faster than flip-flopssince theydon't need to wait for a clock signal.Hence, they are very commonly used in high-speed designs. They also require less power, which is the main intention of our project. Latch-based designs also consume smaller die area.

B. WHY LOW PHASE TRIGGERING?

All the latches used in the control circuitry i.e., the Address latch and the Memory Enable latch are low phase latches. One of the main reasons is to reduce the power consumption. Negative level triggering only does discharge of the capacitors thereby resulting in more power saving while, positive edge triggering only charges the capacitor. Low phase latch is also used to reduce the delay and prevent corruption of information.

C. SEM LATCH USNG SCHMITT TRIGGER CIRCUIT

Soft errors often occur in currentlow-power, high-densityVLSI designs. They are caused by radiation triggered transient pulses produced by alpha particles in the packaging substance and neutrons from cosmic rays[3]. Generally, the working of VLSI circuits isgravely affected by thesoft errors transpiring on the memory systems in logicalcircuits. Therefore, this calls for soft error masking circuits to eliminate these soft errors. This is done by radicallyscaling down the magnitude of the transient pulses along with avery minute penalty in performance.

As shown in Fig. 6, Schmitt trigger circuits exhibit hysteresis property. This means that the Schmitt trigger circuithas two threshold voltages:Vth+ (which is the rising threshold voltageinput) and Vth- (which is the falling threshold voltageinput). Only when the voltage value of the input is greater than Vth+, the output will change from low to high.Similarly, when the input voltage value is lesser than Vth-, the output will change from high to low. Thus, Schmitt trigger circuits can discard a broad spectrum of noise. The input signal '0' along with noise whose value is lower than Vth+ will not appear at output [3]. So, we'll get a proper '0' at the output. Correspondingly, the input signal '1' with noise whose value is larger than Vth- will also not appear at the output and hence giving a proper '1'.

The Schmitt Trigger circuit is used in the construction of the D latch because of its soft error masking property. This latch has been used in our control circuitry as the Address latch and the Memory Enable latch. Fig 7 shows the D latch using a Schmitt trigger circuit. It comprises of a Schmitt trigger circuit along with 2 pass transistors named A and B. Let us assume that there is a logic LOW (0) signal with a transient noise pulse at the input to the proposed latch. First and foremost, the pass transistor named 'A' willdecrease the transient

noise pulse'speak voltage by approximately 10 percent. Following this, the Schmitt trigger circuit portion, which forms a Schmitt trigger buffer, will reduce it further. The Schmitt trigger buffer circuit can mask the soft error only if the peak voltage of the transient noise pulse which is input to the Dlatch is reduced below Vth+ value by the pass transistor A.Similarly, we can explain the circuit working for logic HIGH (1) input signal with transient pulses.

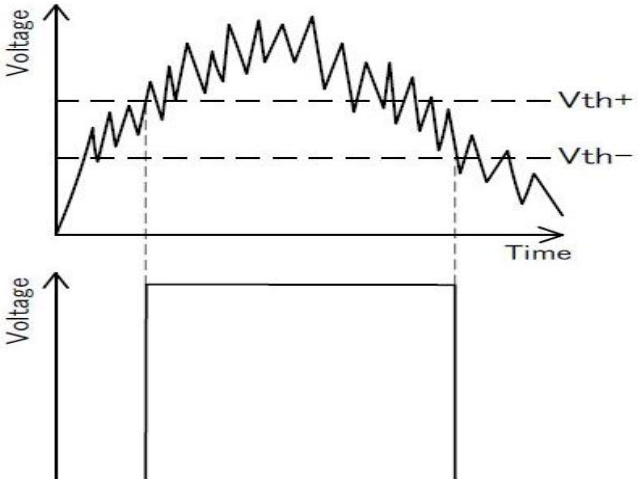

Fig. 6: Schmitt Trigger Waveform

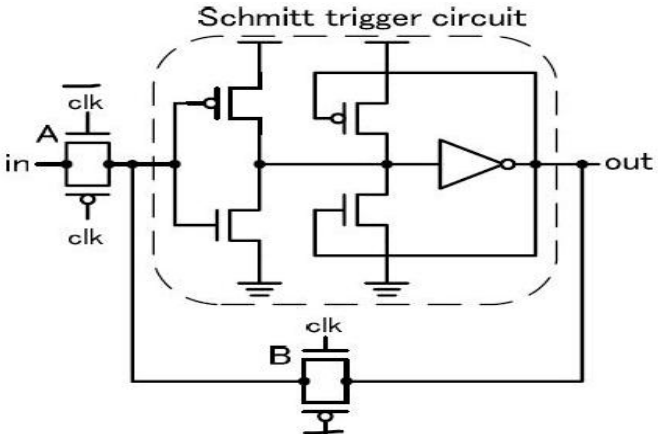

Fig. 7: SEM latch using Schmitt trigger

VI. Comparison of Various Decoders And Latches

A. COMPARISON OF DECODERS

The comparison of various decoders has been done in Table 1. The comparison has been done based on power consumed at different voltages, the number of transistors, delay and PDP (Power-Delay Product). It is seen that the NOR array decoder has the highest power consumption. This is due to large the amount of leakage currents produced by the pass transistors used in the circuit. The delay and PDP of NOR array decoder are also maximum compared to the other two decoder circuits.

The AND gate-based decoder has the maximum number of transistors i.e. 28 and hence will have the maximum area usage compared to the other two decoders. The power consumption and PDP is intermediate to that of the NOR array and Mixed logic decoders. Also, the delay is least compare compared to the rest.

The Mixed logic line decoder uses only 14 transistors, thus having the least area. The power consumed is also minimal compared to the other two decoders. The delay is comparable to the AND gate-based decoder. It can also be clearly seen that the PDP (Power-Delay Product) of Mixed logic line decoder is the least compared to the others. There is about 61% improvement in the PDP as compared to the decoder using AND gates. Due to all these reasons, we have implemented our decoder using Mixed logic.

Table 1: Comparison of various decoders

Decoder Type	Power Consumed(µw)			No. of Transistors	Delay (ns)	PDP (mW)
	2V	1.8V	1V			
2:4 NOR Array decoder	3436	2532.64	317.8134	20	0.745	1886.82
2:4 decoder using AND gates	89.7366	71.0041	19.5787	28	0.1147	8.1442
Mixed Logic 2:4 Line Decoder	18.4921	14.8445	4.1249	14	0.214	3.1767

B. COMPARISON OF LATCHES

Table 2: Comparison of various latches

Latch type	Power consumed (µW)			No. of transistors	Delay (ns)	PDP (mWs)
	2v	1.8v	1v			
8T Latch	121.0062	86.7217	-	8	0.83276	69.7201
6T Latch	116.3989	84.5721	0.4206	6	0.08695	7.3535
Tri state buffer Latch	41.9688	33.0729	8.7589	10	0.19728	6.5246
TG Latch	20.4845	25.5479	5.7258	10	0.08219	2.0998
SEM Latch using Schmitt trigger circuit	32.1549	25.7622	7.2064	10	0.08904	2.2939

The comparison of various latches based on various factors was done. The factors include the number of transistors, the power consumed at various voltages, the delay of the circuit as well as the PDP (Power-Delay Product). Table 2 shows a comparison of them. From the table, we can see that 8T and 6T latches even though having less number of transistors have a high power consumption and delay. They also are not very robust. They lose their functionality at low voltages (from 1V for 8T latch). So, these latches couldn't be used in our design. The tri-state buffer latch, TG (conventional Transmission Gate based latch) latch and SEM latch all have the same number of transistors. However, the tri-state buffer latch has more delay and power consumption compared to the other two. The TG latch, and SEM latch have almost comparable PDP values, but we finally used SEM latch instead of TG latch because of its soft error masking property.

VII. Simulation Results

A. GATED CLOCK

The gated clock has been implemented using a simple CMOS AND gate. The schematic of the AND gate can be seen in Fig. 8. In this, a symbol of NOT gate or inverter has been used which can be seen as a rectangle. The simulated waveform is shown in Fig. 9. The first wave represents the Memory Enable signal, the wave is the clock signal and the third is the output of gated clock. As can be seen from the figure, only when enable is on, the clock signal is passed to the output. The powerconsumption of this AND gate was found to be 94.33 nW for power supply of 1.2V. The delay was found to be 0.24 ns.

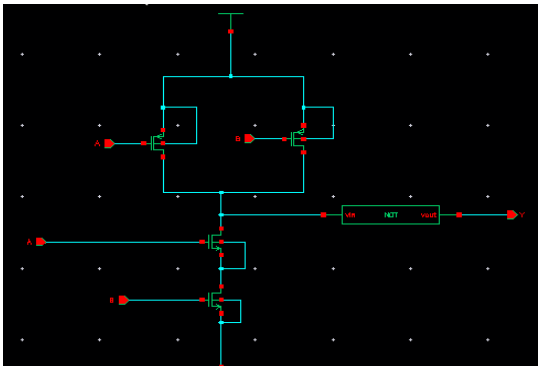

Fig. 8: Schematic of gated clock

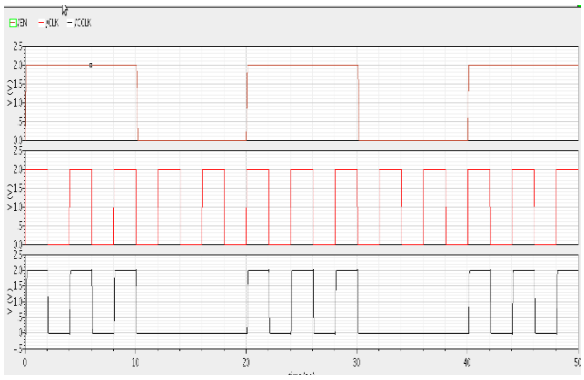

Fig. 9: Waveform of gated clock

B. DECODER

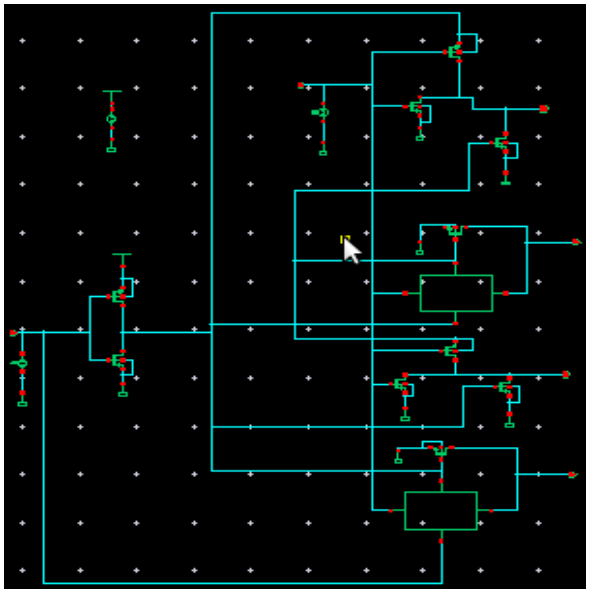

Fig. 10: Schematic of Mixed logic 2:4 line decoder

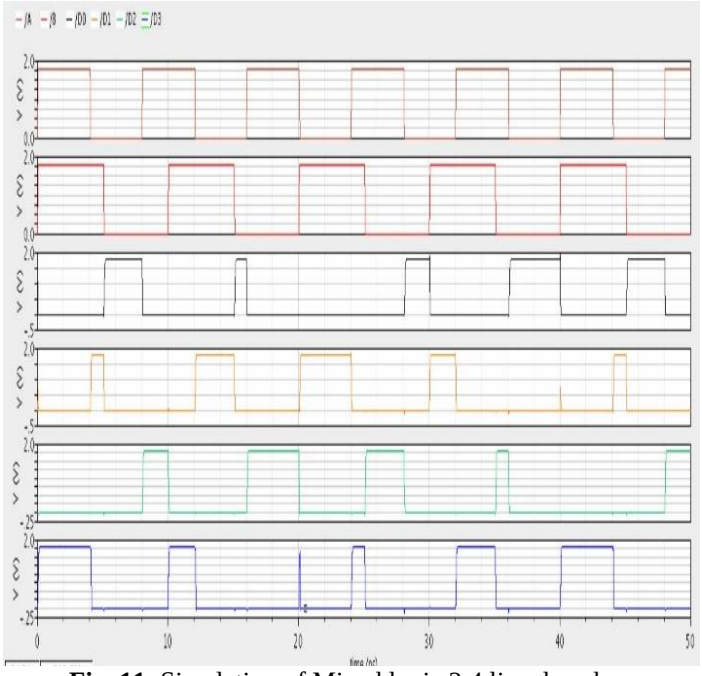

Fig. 11: Simulation of Mixed logic 2:4 line decoder

Fig. 10 shows that schematic of 2:4 mixed logic line decoder. The rectangular symbol represents a transmission gate. The simulated waveform is shown in Fig. 11. The first two waveforms indicate the inputs A and B to the decoder. The next four waves represent outputs D0, D1, D2, D3. From the waveform, we can see that when both inputs are low, D0 is activated. When both the inputs are high, D3 is high. When A=1 (high) and B=0 (low), D2 is activated and when A=0 (low) and B=1 (high), D1 is activated. The power consumed by the mixed logic 2:4 line decoder was calculated to be 4.1249 µW at 1 V supply voltage. The critical path was found to be D0 with a delay of 0.214 ns. The PDP of this decoder was found to be 3.1767 mW.

The schematic of 7:128 decoder with gated clock is shown in Fig. 12. The simulation of the 7:128 decoder can be seen in Fig. 13.

As can be seen from the simulation in Fig. 10.7, D27 gets activated when input 0011011 is given. Here A6 represents MSB and A0 represents LSB. The total power consumed by the 7:128 decoder at 1 V power supply is 0.398 mW. The critical path of this decoder was also found. The critical path was D3 with a delay of 0.609 ns.

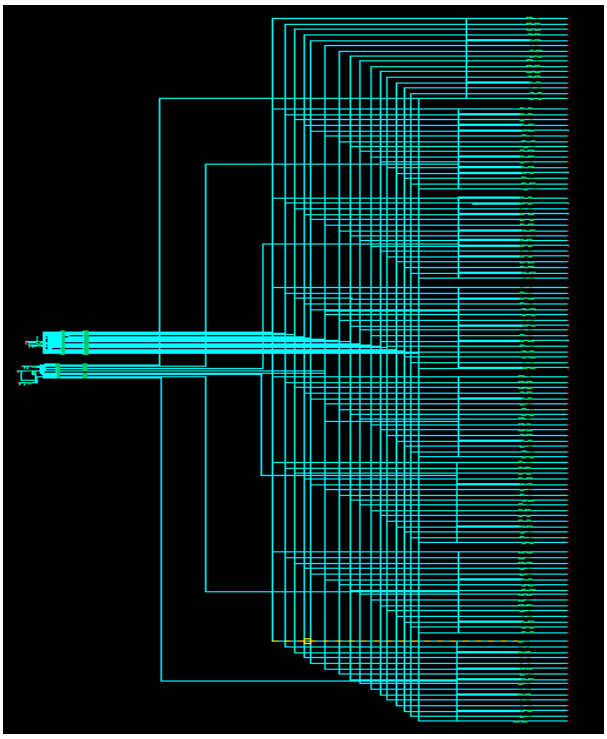

Fig**. 12**: Schematic of 7:128 decoder

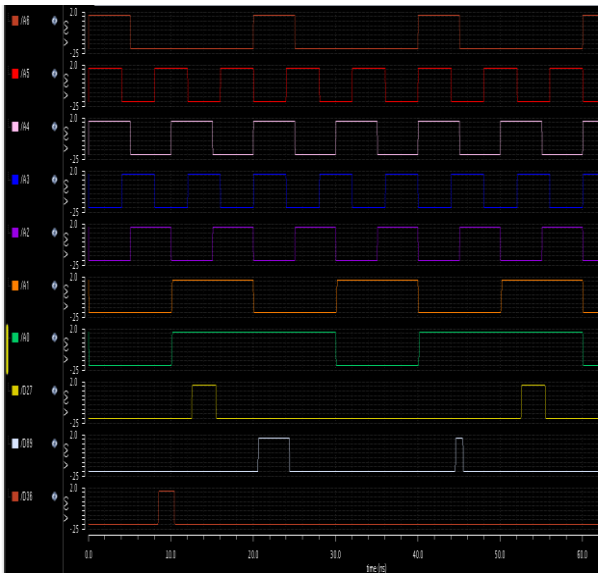

Fig. 13: Simulation of 7:128 decoder with gated clock

C. LOW PHASE SEM LATCH

Fig. 14 is the schematic of SEM latch using Schmitt trigger circuit. The inverter is represented using a rectangular symbol. The simulated waveform of this SEM latch is shown in Fig. 15. This circuit consumed 7.2064 µW at a power supply of 1 V. The delay of this circuit is 0.08904 ns. The SEM latch using Schmitt trigger circuit had 65% improvement in PDP over the tri-state buffer latch.

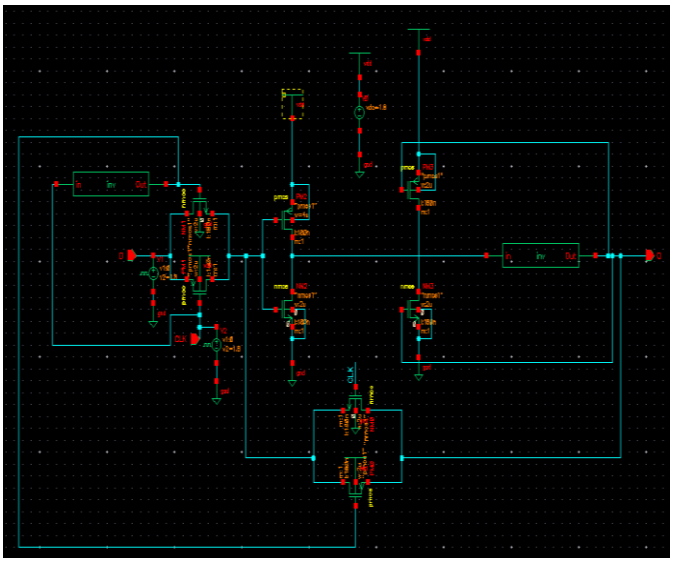

Fig. 14: Schematic of SEM latch

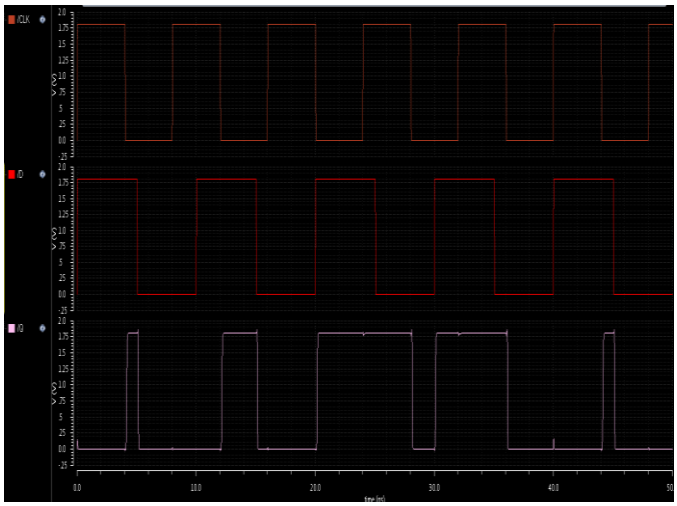

Fig. 15: Simulation waveform of SEM latch

D. Control Circuitry

The entire schematic of the control circuitry can be seen below in Fig. 16. The long vertical block is the wordline decoder and the horizontal block is the column decoder. The latches can also be seen beside the decoders. Clock gating can also be seen given to the latches as well as the decoders.

Fig. 17 shows the schematic waveforms of the control circuitry. The first 7 waveforms are the inputs A0-A7. The penultimate waveform which is shown in yellow is the output of the wordline decoder and the last waveform in grey colour is the column decoder output. For simulation, the same inputs have been given to both the wordline and the column decoder. It can be seen from the simulation that when all inputs are high the W127 is high i.e. the last wordline is high. The B8 bitline is high when input is 0001000. The overall power consumption of the control circuitry was found to be 1.5675 mW and the delay was 0.711 ns.

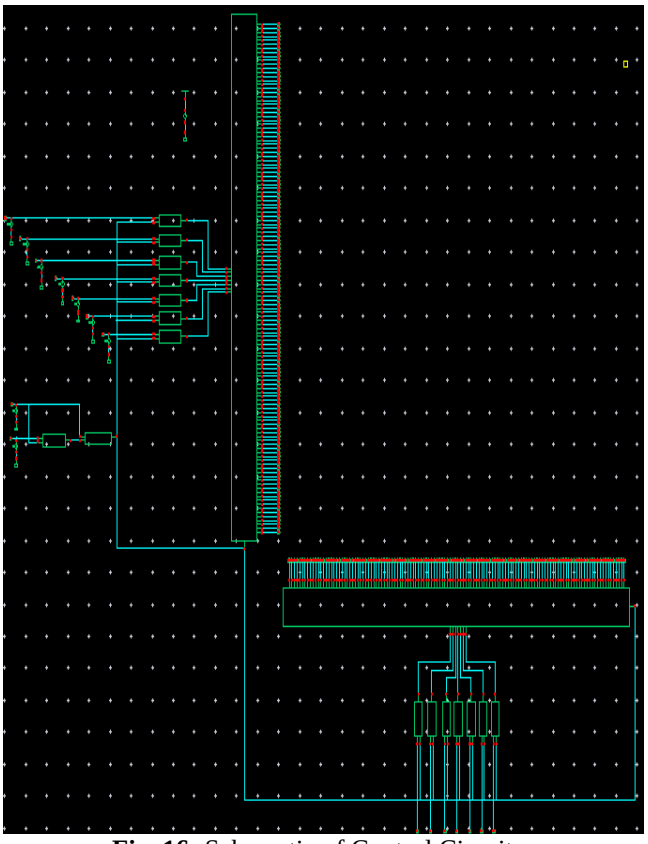

Fig. 16: Schematic of Control Circuitry

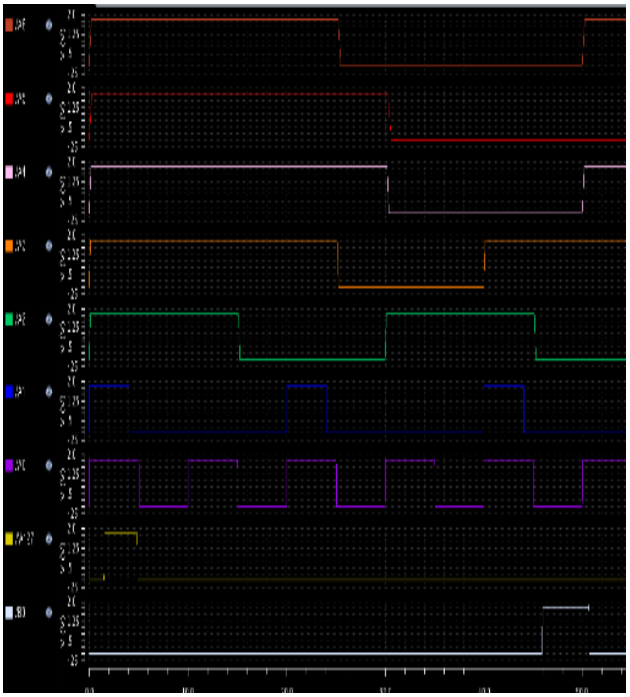

Fig. 17: Simulation waveform of Control Circuitry

VIII. Conclusion

The proposed paper involves reducing the power consumption in the control circuitry which is a very important part of the ROM architecture. The control circuitry is involved in fetching the address location to be read and activating the particular wordline and bitline. All the designs and analyses were done using Cadence 180nm technology and LTspice tools. We have introduced clock gating to reduce the power consumption. A unique feature introduced is that, we have incorporated gated clock in the design of decoder. This was done to

further reduce power consumption even though the decoder is a combinational circuit and doesn't need a clock signal. We have done a detailed comparison of various decoders and latches and the ones with the best features have been implemented in our design of the control circuitry. Battery life has become one of the most important denominators while choosing an electronic device. Reducing the power leads to cost reduction. It will also help save the environment. Through this paper we have worked to reduce the power consumption which is major factor in today's world of growing technology where people want their devices to last for a longer duration.

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Riya Dey"Implementation of Control Circuitry for Ultra-Low Power ROM" IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) 14.4 (2019): 27-38.